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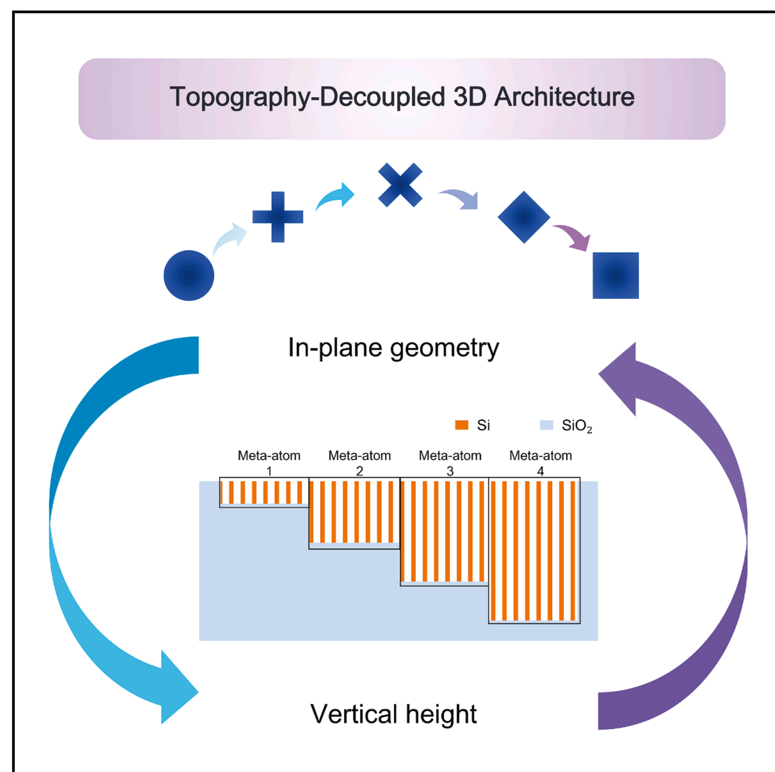
Wafer-scale topography-decoupled 3D metasurfaces

Graphical abstract



Highlights

- Topography-decoupled strategy enables wafer-scale 3D metasurface manufacturing
- Multi-cycle lithography etching and CMP yield 2.2-nm wafer-level height precision
- A 46,072-unit combinatorial library enables deterministic structure-color mapping
- 3D metasurface yields 78.2% sRGB gamut, overcoming planar limits under the same constraints

Authors

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In brief

Chen et al. present a topography-decoupled manufacturing strategy that integrates chemical mechanical polishing with multi-cycle lithography and etching to construct multi-level 3D silicon nanostructures. Validated through a massive 46,072-unit structural library, this platform achieves 78.20% sRGB gamut coverage. The realization of 3D metasurfaces on a 4-inch wafer demonstrates the feasibility of large-scale batch processing for next-generation nanophotonics.

Explore
Early prototypes with exciting performance and new methodology

Chen et al., 2026, Device *4*, 101118
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https://doi.org/10.1016/j.device.2026.101118

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Please cite this article in press as: Chen et al., Wafer-scale topography-decoupled 3D metasurfaces, Device (2026), https://doi.org/10.1016/j.device.2026.101118

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Wafer-scale topography-decoupled 3D metasurfaces

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https://doi.org/10.1016/j.device.2026.101118

THE BIGGER PICTURE Achieving optical performance with a compact footprint is in demand for a diverse range of emerging applications, such as AR displays and miniaturized cameras. Planar metasurfaces use flat arrays of subwavelength structures to integrate complex optical functionalities, such as wavefront shaping and polarization control, onto sub-millimeter chips. However, planar metasurfaces are constrained by the single lithographic layer, which forces trade-offs between optical efficiency and bandwidth. Transitioning to three-dimensional (3D) architecture can overcome these physical bounds by utilizing varying structural heights as an additional degree of freedom. Yet mass-producing such 3D nanostructures remains a challenge due to uneven topography during multi-level fabrication. In this work, we introduce a scalable manufacturing paradigm that transforms complex vertical profiles into stacked, planarized layers, enabling the robust mass production of high-performance 3D meta-optics.

SUMMARY

Metasurfaces offer design freedom and compact morphology for next-generation integrated photonics. Yet the optical performance of planar architectures is bounded by the structural degrees of freedom within the single lithographic layer. Three-dimensional (3D) height modulation offers a pathway for independent phase and spectral manipulation, but its realization is impeded by fabrication efficiency, precision, and process incompatibility with standard lithography. In this work, we report a wafer-scale topography-decoupled manufacturing technique. By integrating chemical mechanical polishing (CMP) into a multi-cycle overlay process, the construction of vertical profiles is resolved into a superposition of planarized two-dimensional (2D) patterning steps. The efficacy of this platform is validated on a 4-inch fused silica wafer, achieving precise height control with a standard deviation of 2.2 nm. A combinatorial library containing 46,072 silicon nanopillar metasurface units is constructed, demonstrating an expanded sRGB gamut coverage of 78.20%, representing a 20.7% enhancement over planar architecture.

INTRODUCTION

Metasurfaces in photonics can manipulate optical wavefronts through subwavelength nanostructures.[1–6] For example, planar two-dimensional (2D) metasurfaces can provide functionalities including wavefront shaping, polarization control, advanced display,[7–11] and silicon-based optoelectronic devices.[12–16] The optical performance of these planar architectures is constrained by the geometric degrees of freedom available within a single lithographic layer.[17–21] Phase accumulation, resonance quality factor, and spectral response are coupled to the lateral dimensions of the meta-atoms, which leads to a trade-off between optical efficiency and bandwidth, limiting the accessible parameter space.[22] A transition from planar to three-dimensional (3D) architectures can help overcome these physical bounds and achieve independent control over multiple optical properties.[23,24]

3D architectures can retain the lateral geometric design flexibility, while the vertical dimension introduces a critical degree of freedom that decouples spectral positioning from resonance strength. One approach is grayscale electron-beam lithography (EBL), which has been employed to fabricate continuous-profile diffractive optical elements (DOEs).[25–27] However, this method

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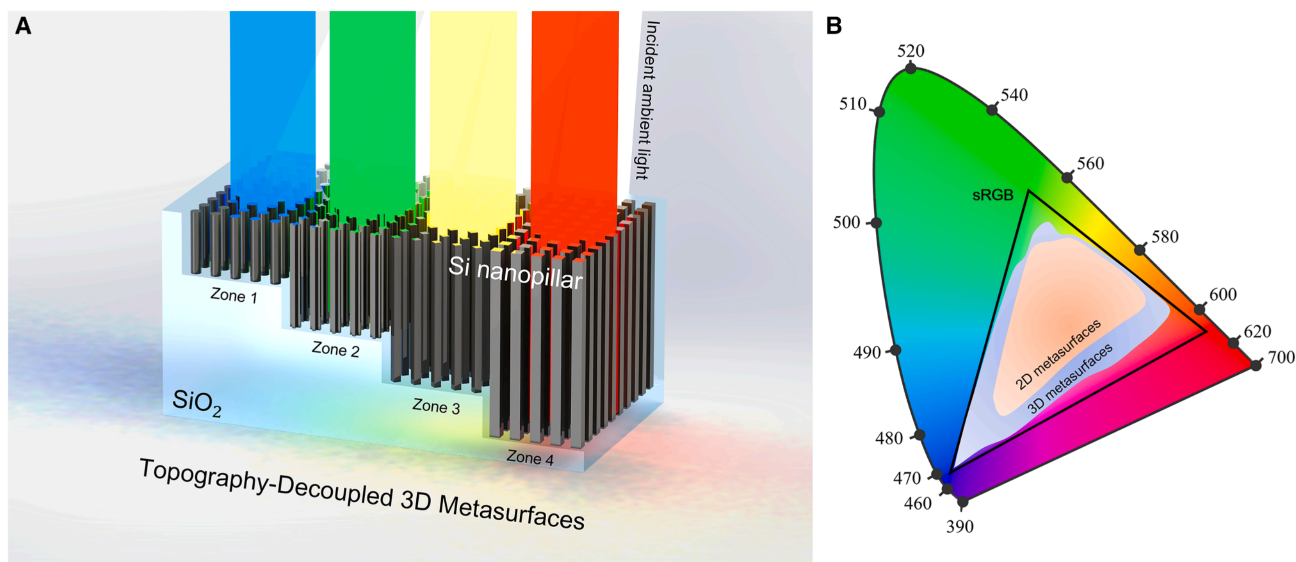

Figure 1. Schematic of topography-decoupled 3D metasurfaces

(A) Working principle showing optical modulation via simultaneous control of in-plane geometry and structural height.

(B) Comparison of optical performance between 2D and 3D metasurfaces on the CIE 1931 chromaticity diagram under identical fabrication constraints.

relies on the nonlinear sensitivity of the resist to exposure dose, which often results in deviations from the intended structural profile and poor control over discrete vertical steps, degrading the performance of resonant metasurfaces. Another technique is two-photon polymerization (TPP) 3D printing.[28–32] While TPP excels at creating complex freeform scaffolds, it is predominantly restricted to polymer-based materials with low refractive indices ($n \approx 1.5$). This presents a disadvantage compared to high-refractive-index semiconductor platforms, as the low refractive index contrast fails to support strong Mie resonances or tight optical confinement. Structural depth modulation through ultrafast laser fabrication on silica substrate[33] and internal 3D processing within transparent materials[34] have been demonstrated as alternative nanofabrication routes. However, these direct-writing methodologies are constrained by restricted throughput and the difficulty in achieving high-index contrast with nanometer-scale precision across wafer-scale areas. To circumvent the limitations of direct 3D processing, discrete layer-by-layer fabrication has emerged as an alternative. For instance, attempts have been made to fabricate multi-layer dielectric metasurfaces through iterative stacking.[35–38] However, this method introduces alignment errors and interfacial losses. Similarly, strategies utilizing multi-cycle lithography have been implemented to realize zonal height modulation within homogeneous silicon carbide substrates for augmented reality (AR) display applications.[39] Yet, without surface planarization, the accumulated topography from underlying layers creates unevenness, leading to depth of focus issues and misalignment that prevent scaling to large areas.

In this work, we present a wafer-scale fabrication paradigm rooted in the topography-decoupled principle (see Figure 1). By integrating chemical mechanical polishing (CMP) into a multi-cycle overlay process, the construction of vertical profiles is resolved into a superposition of planarized 2D patterning steps. Distinct from conventional multi-level DOEs that rely on vertical height discretization for phase approximation, this architecture integrates the vertical dimension as an independent modulation channel alongside in-plane nanostructuring. Such a configuration enables the manipulation of both geometric morphology and structural height at the individual meta-atom level. The optical advantages of the 3D architecture are quantified by constructing a library containing 46,072 structural units distributed across four distinct structural heights. An expanded sRGB gamut coverage of 78.20% is realized, representing a 20.7% enhancement over the limits of planar counterparts. A direct and deterministic mapping from design targets to fabrication parameters is established. The efficacy of this platform is validated through the fabrication of multi-level silicon metasurfaces on a 4-inch fused silica wafer. The scalability and precision of the process are evidenced by the realization of wafer-scale color pixel arrays, confirming the capability of this method for the high-fidelity manufacturing of next-generation meta-optics.

RESULTS AND DISCUSSION

Combinatorial structural design library

To evaluate the manufacturing fidelity and versatility of the topography-decoupled platform, a combinatorial structural design library was established. Rather than being limited to a specific functional device, this approach enables an assessment of the fabrication capability across a broad parameter space. Silicon nanopillars patterned on a fused silica substrate were employed as building blocks, leveraging the high refractive index contrast to facilitate localized optical resonances. As illustrated in Figure 2, five distinct geometric morphologies, comprising circle, square, cross, rhombus, and x-shape, were selected to

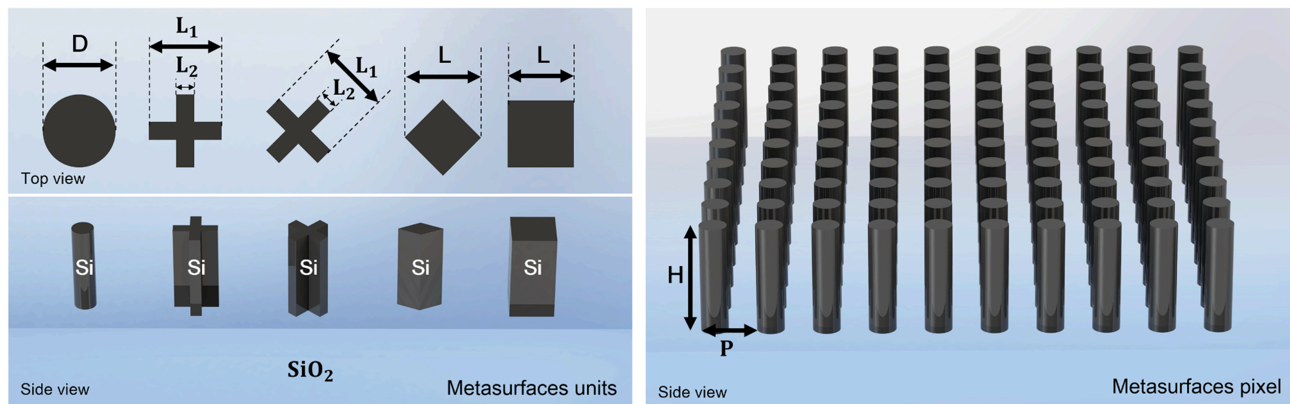

Figure 2. Configuration of the combinatorial structural design library

diversify the accessible optical modes and to serve as geometric benchmarks for evaluating lithographic fidelity. These meta-atoms were organized into periodic arrays to constitute metasurface pixels, wherein the optical response is governed by the geometric parameters defined by the lattice period (*P*), the lateral critical dimension (*D* or *L*), and the structural height (*H*). In contrast to conventional planar metasurfaces, where the height is fixed to a single value, the vertical dimension in this design was exploited as a control variable to validate the process versatility in handling multi-level topography.

A high-density combinatorial dataset was constructed to explore the fabrication parameter space. The structural height was modulated across four distinct levels to introduce varying degrees of vertical phase accumulation and aspect ratios. By traversing the lateral dimensions and scaling factors across the five geometric types while varying the height, a vast array of structural combinations was generated. This design library functions as a large-scale test matrix, allowing for the statistical assessment of fabrication precision across multi-level topography. This approach demonstrates that the introduction of height modulation expands the available structural degrees of freedom. A universal hardware basis for diverse nanophotonic applications is provided, extending beyond the physical limits of single-layer architectures.

Height-modulated spectral engineering

To quantify the spectral modulation capability enabled by the additional vertical degree of freedom, silicon nanopillar metasurfaces were fabricated on fused silica substrates. Five distinct geometric morphologies, comprising circle, square, cross, rhombus, and x-shape, were employed as the building blocks to diversify the optical resonance modes. The design library was divided into 886 structural zones, with each zone occupying a $12 \times 12\ \mu m^2$ area. To cover the parameter space, the lattice periods were discretized into four variants of 400, 500, 600, and 700 nm. The lateral critical dimensions were swept to yield duty cycles ranging from 20% to 80%. To explore the parameter space within the fabrication limits, 13 scaling factors ranging from 0.4 to 1.0 were applied to these base designs. These variations were implemented across four structural heights of 100, 130, 160, and 190 nm. These structural heights were determined through numerical simulations to ensure that the resulting geometries cover the critical aspect ratio range required to support the fundamental resonance modes across the visible spectrum. This combination resulted in a test matrix containing a total of 46,072 unique structural combinations. Beyond serving as a benchmark for fabrication fidelity, this experimental dataset establishes a direct and deterministic mapping between 3D geometric parameters and the resulting optical chromaticity. In contrast to conventional design workflows, which rely on numerical simulations followed by iterative process calibration to compensate for fabrication deviations, the specific structural configurations required for a targeted color coordinate are retrieved directly from this empirical library. A look-up table retrieval algorithm was implemented. Upon defining a target chromaticity coordinate in the CIE 1931 diagram, the algorithm scans the empirical library to identify the structural unit that yields the minimum color difference. The corresponding fabrication parameters (*P*, *D*, *L*, and *H*) are then extracted from this optimal match. This procedure enables the direct acquisition of pre-calibrated geometric definitions for the desired optical response.

The fabrication quality and optical response of the prepared samples were characterized. Optical micrographs of the metasurface arrays corresponding to the four silicon height groups are presented in Figure 3A, where the subset with a scaling factor of 1.0 is selected for demonstration. Pronounced chromatic shifts dependent on the structural height are manifested across the arrays, confirming the efficacy of the height-modulation strategy. To verify the geometric fidelity of the fabrication process, the top morphology of the nanostructures was examined via scanning electron microscopy (SEM). As shown in Figure 3B, high-fidelity pattern definition and sharp structural features were achieved for all five geometric shapes, ensuring that the characterized optical variations are attributable to the intended design parameters rather than fabrication defects. To enable high-throughput extraction of color information from the high-density array of fabricated structures, a charge-coupled device (CCD)-based imaging technique was employed. The chromaticity coordinates were derived from the calibrated images and visualized on the CIE 1931 chromaticity diagram, as presented in Figure 3C. The color gamut occupancy within the sRGB standard space was analyzed. The coverage ratios for

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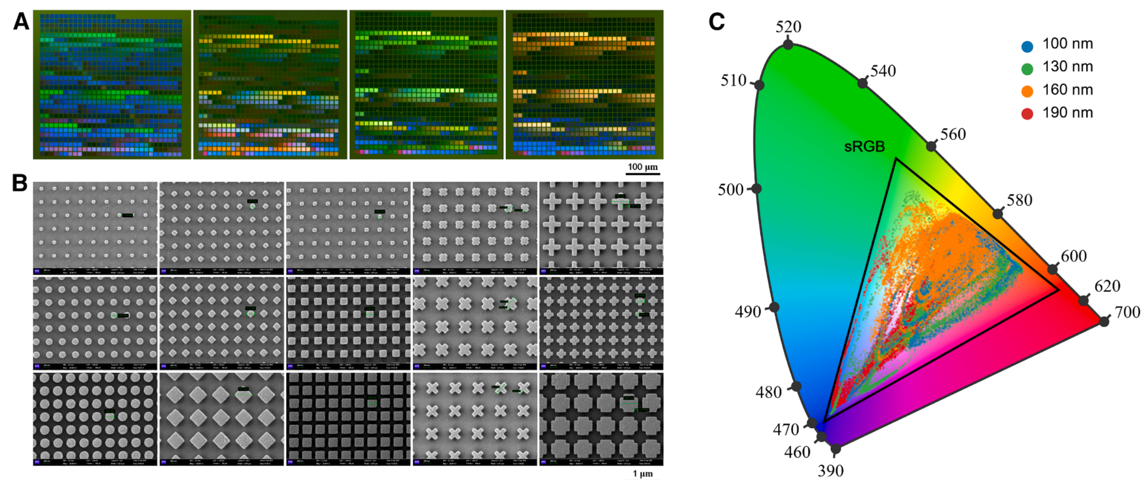

Figure 3. Optical characterization of the 3D metasurfaces

(A) Microscope images of silicon 3D metasurfaces arrays with structural heights of 100, 130, 160, and 190 nm.

(B) SEM images of the five metasurfaces unit geometries with varying duty cycles.

(C) The measured spectral distribution for the four structural height groups in CIE 1931 chromaticity diagram.

the single-height groups were calculated as 46.05%, 64.78%, 46.58%, and 41.21% for structural heights of 100, 130, 160, and 190 nm, respectively. By integrating these distinct height-modulation channels, the collective gamut coverage of the 3D metasurfaces was expanded to 78.20%. This result represents a relative enhancement of 20.7% compared to the maximum coverage achievable with the optimal single-height configuration, demonstrating that the topography-decoupled strategy circumvents the spectral saturation limits in planar architectures.

Wafer-scale topography-decoupled 3D metasurface fabrication

A wafer-scale fabrication workflow compatible with standard complementary metal-oxide-semiconductor (CMOS) infrastructure is proposed. This scheme was implemented to fabricate 14 die structures on a 4-inch fused silica wafer, exemplified by the realization of high-fidelity 3D metasurface color pixels.

The fabrication workflow for the 3D metasurfaces is illustrated in Figure 4A. Global alignment marks were defined via contact photolithography followed by a lift-off process. Recessed structural zones with spatially varying depths were subsequently patterned through multi-cycle photolithography combined with inductively coupled plasma (ICP) etching. A silicon layer was then deposited to fill the structural cavities through plasma-enhanced chemical vapor deposition (PECVD), after which the surface was planarized and thinned using CMP and ICP etching. Finally, the lateral structural patterning was completed by EBL, and the metasurfaces featuring four distinct structural heights were realized through the corresponding multi-cycle photolithography and ICP etching steps.

The resulting 4-inch fused silica wafer, fabricated using this topography-decoupled strategy, is presented in Figure 4B. Two distinct color pixel configurations were realized: a 5×5 pixel array with a 2.8×3.5 mm pattern area and a 7×7 pixel array with a 2.9×3.9 mm pattern area, both consisting of individual pixels measuring 12×12 μm^2. Optical microscopy inspection revealed color uniformity and repeatability across the arrays, consistent with theoretical expectations. To evaluate the film quality on a macroscopic scale, the silicon film thickness was characterized at nine points ranging from the wafer center to the periphery using an ellipsometer. As shown in Figure 4C, a standard deviation of 2.2 nm was obtained for the silicon film thickness, validating the wafer-level uniformity achieved by the planarization process.

The lateral morphology and vertical profile of the fabricated structures were characterized using critical dimension SEM (CDSEM) and atomic force microscopy (AFM), respectively, with the results presented in Figure 4D. The CDSEM images confirm that the lateral geometry of the 3D metasurfaces is well-defined and aligns with the design patterns. AFM measurements performed on four representative structural height groups yielded vertical dimensions of 88.54, 113.18, 138.99, and 153.30 nm. The observed deviations from design values are primarily attributed to pattern-dependent loading effects during the ICP etching process and tip convolution artifacts inherent to AFM measurements in narrow trenches. While depth-control precision can be optimized through cross-sectional SEM calibration of sacrificial samples, the combinatorial library strategy employed herein exhibits robustness against systematic errors. By mapping the measured optical response of fabricated structures, the workflow accommodates geometric biases, bypassing the stringent requirement for absolute fabrication fidelity. These distinct height values confirm that the targeted multi-level distribution was realized, demonstrating the capability of the method to achieve zonal height control.

Conclusion and outlook

The 3D metasurface fabrication scheme proposed in this work adopts processing technologies fully compatible with semiconductor fabrication. Since the scale of metasurface structures

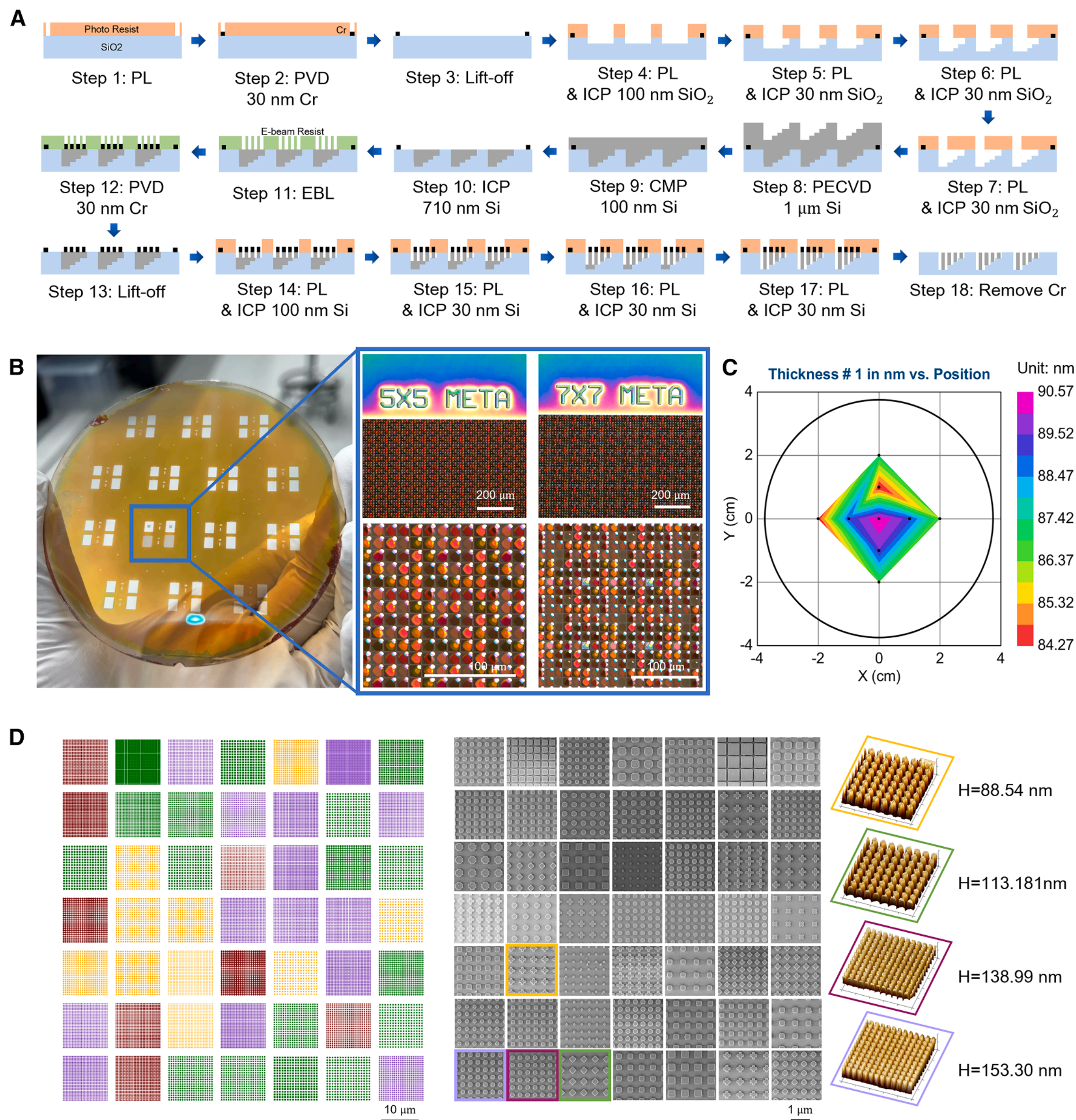

Figure 4. Wafer-scale fabrication and characterization of topography-decoupled 3D metasurfaces
(A) Flowchart of the CMOS-compatible fabrication process.
(B) Photographic image of 4-inch quartz wafer containing 14 3D silicon metasurface dies. The insets display micrographs of the 5 × 5 and 7 × 7 pixelated 3D metasurface arrays.
(C) Silicon film thickness uniformity measured by ellipsometer.
(D) Height distribution map (left) and CD SEM images with corresponding AFM profiles (right) for the four structural heights (100, 130, 160, and 190 nm).

lies in the nanometer range, traditional macroscopic machining is inapplicable, necessitating the adoption of IC processing methods. While applying these mature processes enables high-precision batch fabrication over large areas, a challenge persists: optical metasurfaces require the complete filling of nanostructures with various duty cycles, a requirement that is distinct from logic devices. Under identical processing conditions, the simultaneous control of in-plane morphology and cross-sectional profile increases nanofabrication difficulty, a factor that has confined structural processability to 2D architectures. Here, this limitation is overcome by the topography-decoupled strategy, which bridges the gap between photonic design requirements and standard foundry capabilities.

In contrast to this topography-decoupled paradigm, alternative 3D manufacturing methods face intrinsic limitations. With the development of TPP, fabricating nanoscale 3D structures using organic photoresists enables freeform scaffolding. However, these materials typically possess low refractive indices, hindering high-performance optical device preparation. Furthermore, TPP precision is inferior to EBL, deep ultraviolet (DUV)

lithography, or nanoimprint lithography (NIL), and its low processing efficiency precludes wafer-scale batch fabrication. Similarly, stacking multiple 2D metasurface layers suffers from interfacial energy losses and unresolved issues regarding system complexity, volume, and weight. Unlike these approaches, the proposed method ensures material performance and structural fidelity without such trade-offs.

The proposed manufacturing workflow is compatible with standard IC foundry protocols, enabling automated, batch-level production. The lithography techniques can be tailored to specific resolution and scale requirements. For micron-scale features, cost-effective contact photolithography suffices, whereas high-precision EBL or DUV steppers are employed for nanoscale definitions. The planarization achieved via CMP facilitates the adoption of NIL for high-fidelity structure transfer, enabling the low-cost replication of complex morphologies such as slanted gratings. Beyond standard geometric primitives, this topography-decoupled paradigm accommodates topology-optimized meta-atoms. Because the in-plane morphology is delineated by high-resolution lithography, the definition of features typically generated via inverse design algorithms is supported, extending the structural library beyond standard geometric primitives. The platform also supports vertical scalability. Although the present four-level configuration reflects a strategic compromise between performance and yield, aspect ratios exceeding 10:1 within a 1 μm range should be attainable. Extending height levels to augment optical manipulation is also feasible, constrained primarily by process complexity. From a physical perspective, the vertical dimension decouples phase accumulation from scattering amplitude by modulating optical path length at a constant fill factor. This mechanism circumvents the efficiency-bandwidth trade-off inherent to planar designs, where lateral scaling couples resonance strength to geometric size.

While numerical simulations frequently predict wider gamuts, experimental realizations are often constrained by fabrication imperfections.[40,41] In contrast, the performance reported herein is derived from a dataset of 46,072 characterized structural units. This empirical validation accounts for process deviations, establishing 78.2% as a wafer-scale realizable standard for all-dielectric silicon metasurfaces.

To extend this paradigm to phase-only meta-optics, particularly achromatic meta-lenses, one may exploit the vertical dimension as an independent phase compensation channel. This can alleviate lithographic constraints on lateral critical dimensions, enabling the maximization of achromatic bandwidth and focusing efficiency while circumventing the fabrication complexity of high-aspect-ratio nanostructures. However, the current workflow is limited by pattern-dependent loading effects during etching, which introduce morphological variations across different structural geometries. Future research could integrate fabrication compensation algorithms to co-optimize optical design and process parameters, minimizing these manufacturing-induced performance discrepancies. This work establishes a universal hardware foundation for the next generation of meta-optics, paving the way for the commercial deployment of advanced nanophotonic applications, including holographic displays, optical encryption, and ultra-compact sensors, and potentially extending to active tunable metasurfaces and heterogeneous material integration within standard semiconductor infrastructure.

METHODS

High-throughput color analysis

To enable rapid and high-throughput characterization of the structural colors across the massive metasurface array, an automated image analysis pipeline was developed based on optical microscopy. The entire sample was first imaged using a calibrated optical microscope equipped with a color CCD camera under uniform, diffuse white-light illumination.

The raw micrograph, which contains a grid of 30×30 individual metasurface pixels per structural zone, was then processed algorithmically. For each pixel, a small region of interest (ROI) centered on the pixel was extracted. The average RGB value within this ROI was computed to represent the perceived color of that specific meta-atom configuration. To facilitate quantitative analysis and comparison within a device-independent color space, these sRGB values were converted to CIE 1931 chromaticity coordinates (x,y) using a standardized colorimetric transformation. This process involved a two-step conversion: first from sRGB to CIE XYZ tristimulus values and subsequently from XYZ to the xyY chromaticity coordinates. The resulting (x,y) coordinates for all measured pixels were then directly plotted on the CIE 1931 chromaticity diagram to visualize and quantify the achieved color gamut. This automated, image-based approach allowed for the efficient extraction of over 46,000 color data points, providing a comprehensive and empirical mapping between the 3D geometric design parameters and their corresponding optical response.

Materials and fabrication

Commercial 0.5-mm-thick, 4-inch JGDS1 standard silica wafers (Feilihua F-HUV4) were selected as the substrates, while the silicon film was prepared using PECVD (LEUVEN HAASRODE-P200A). Global alignment marks were initially defined on the wafer using a contact aligner (SUSS MA6), followed by the deposition of a 40 nm chromium layer using a physical vapor deposition (PVD) machine (ULVAC ei-5z). The photoresist (Allresist AR-P 5350) and excess metal in the non-exposure regions were removed by immersion in a heated NMP solution (SINOPHARM 872-50-4). Based on these alignment marks, overlay photolithography was performed using the contact aligner, and the silica substrate was etched using an ICP etcher (LEUVEN HAASRODE-E200A) with CHF_3 gas. The etching depth was strictly calibrated using a profilometer (J.A. Woollam RC2).

The overlay photolithography and ICP etching cycle was iterated 4 times to define the recessed structural zones corresponding to 4 distinct structural heights. Subsequently, a 1-μm-thick silicon layer was deposited on the top of the wafer using a PECVD system. Surface planarization was carried out using a CMP system (GNP POLI-500), effectively reducing the topographic variations derived from conformal growth. To ensure precise endpoint detection during the subsequent thinning phase, a multi-cycle ICP etching strategy using SF_6 and O_2 gases was adopted. In each cycle, the etch rate was dynamically calibrated by measuring the residual silicon thickness in

non-structural areas using an ellipsometer. The film thickness within the recessed structural zones was then calculated by correlating these ellipsometric data with the step-height offsets measured via profilometry, thereby ensuring accurate termination at the design target. Once the silicon film reached the design thickness, overlay exposure was executed using an EBL system (Raith EBPG 5150) based on the alignment marks. A 25-nm chromium hard mask was deposited by PVD and formed through a lift-off process to achieve pattern transfer. Finally, the zonal height modulation of the silicon nanopillars was realized through multiple rounds of contact photolithography overlay and ICP etching. The device fabrication was completed by removing the residual chromium mask through chromium etchants (CHANGSHA JINXIN JET-929).

RESOURCE AVAILABILITY

Lead contact

Further information and requests for resources and reagents should be directed to and will be fulfilled by the lead contact, Min Qiu (qiu_lab@westlake.edu.cn).

Materials availability

This study did not generate new unique reagents.

Data and code availability

All data and code supporting the findings of this study are available from the lead contact upon reasonable request.

ACKNOWLEDGMENTS

This research was supported by the National Natural Science Foundation of China (U25A203659, 62325504, 625B2153, 52203305, and U21A20494) and the National Key Research and Development Program of China (no. 2024YFB2809200). 3D metasurface samples were fabricated at Moldnano (Hangzhou) Technology Co., Ltd., and characterized at the Westlake Center for Micro/Nano Fabrication. The authors also acknowledge the Westlake Center for Micro/Nano Fabrication for facility support and technical assistance.

AUTHOR CONTRIBUTIONS

M.Q., T.L., B.C., and Y.C. conceived the idea and initiated the project. Y.C. performed the numerical simulation and structure design. B.C., X.L., and L.C. fabricated the devices. Y.C. and X.L. implemented the optical performance and processed the experimental data. K.D. and D.Z. guided the material characterization and device fabrication. All authors participated in discussions and contributed to writing the paper. All authors confirmed the final paper. M.Q., T.L., and K.D. guided all aspects of the work.

DECLARATION OF INTERESTS

The authors declare no competing interests.

Received: December 29, 2025
Revised: February 10, 2026
Accepted: March 4, 2026

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Please cite this article in press as: Chen et al., Wafer-scale topography-decoupled 3D metasurfaces, Device (2026), https://doi.org/10.1016/j.device.2026.101118

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